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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,054	12/12/2003	Alexandre E. Eichenberger	YOR920030382US1	2495
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HARRINGTON & SMITH, LLP 4 RESEARCH DRIVE SHELTON, CT 06484-6212			EXAMINER COLEMAN, ERIC	
			ART UNIT 2183	PAPER NUMBER
DATE MAILED: 02/09/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/735,054

Applicant(s)

EICHENBERGER ET AL.

Examiner

Eric Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 12-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed program product is not tangibly embodied in a manner so as to be executable. Therefore the claims are directed toward and abstract idea and does not fall into one of the categories of invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aizikowitz (patent No. 5,946,491) in view of Bui (patent No. 6,487, 630).

3. Aizikowitz taught the invention substantially as claimed including a data processing ("DP") system (as per claim 1,12,16) comprising:

a) Introducing a name level instruction for at least one of a named architected register in a processor (e.g., see col. 5, lines 1-48)[spill code instructions are introduced into instruction stream for at least one physical architected register];

b) Allowing a programmer to change the current name level of a register name via said name level instruction (e.g., see col. 5, lines 1-28 and col. 6, lines 8-67)[the level of the register name is changed from the level of the level of the physical register in maximum use to the level of the backing store, because the operation is performed in a programmed computer it is allowed to be programmed in the system by the programmer that writes the program];

c) Memory (120) (e.g., see fig. 1); and

d) Execution unit (110) and registers (112)(e.g., see fig. 1).

4. Aizikowitz did not expressly detail (claims 1,12,16) creating a new register. Bui however taught creating a new register with an internal name and a new name level (e.g., see col. 3, lines 1-67)[a backing store pointer storing the location of the first memory location of the current frame is created and stored in a register]; and Providing a plurality of additional available computer registers (e.g., see col. 3, line 60-col. 4, line 29)[allocates additional physical registers];.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Aizikowitz and Bui. Both reference were directed to the problems of allocating physical registers in a DP system. One of ordinary skill in the art would have been motivated to incorporate the Bui teachings of allocating additional physical registers at least to so the combined system would have registers for newly created

tasks to use in processing even when the almost all the physical registers were previously allocated to processes and some registers were not being used.

6. As per claim 2,3,13 Aizikowitz taught the name level instruction that comprise spill code for spilling data to backing store (e.g., see col. 5, lines 1-28 and col. 6, lines 8-67) and Bui taught spilling of data in registers to backing store using hardware register renaming maintains a pointer to a current physical register for a corresponding architected register (e.g., see col. 3, lines 1-67) Therefore it would have been obvious to one of ordinary skill that in at least one implementation of the Aizikowitz and Bui teachings the name level instruction would have been used for hardware register renaming and would have maintained a pointer to a current physical register for a corresponding architected register.

7. As per claim 4, Aizikowitz taught the name level instruction uses for spilling registers to backing storage (e.g., see col. 1, lines 1-48) Bui taught a register store engine that uses physical registers were organized in a stack for spilling registers to backing store (e.g., see col. 4, lines 45-55) for backing store operation (e.g., see col. 2, lines 50-64). Therefore it would have been obvious to one of ordinary skill that in at least one implementation of the Aizikowitz and Bui teachings the name level instruction would have used a register stack in the spilling of registers to backing store.

8. As per claim 5, 6 Aizikowitz taught the name level instruction uses for spilling registers to backing storage (e.g., see col. 1, lines 1-48). Bui taught the storing register stack engine saves contents of registers in a cache in a stack fashion (e.g, see col. 4, lines 13-23)[the combination of the Aizikowitz name level instruction for implementing

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register spilling and the Bui teaching of spilling of registers to a cache comprises the name level instruction that uses a hardware-managed register cache as the normal operations of a cache are managed by hardware even though some cache operations can be programmed]. Further since the cache in the Bui teaching is used for spilling it performs as a special purpose memory (as per claim 6).

9. As per claim 7, Aizikowitz taught the name level instruction uses a hardware-managed component of a main storage(120) of a system (e.g., col. 5, lines 1-28 and col. 8, lines 10-35).

10. As per claim 8,10,11,14,15 Aizikowitz taught that the name level instruction uses software-managed component of main storage of a system for spilling register contents (e.g., see col. 5, lines 1-28). Since the code spilled to a specific region of main memory would have had have been retrieved upon request for use by a task one of ordinary skill implementing the Aizikowitz teaching would have been motivated to incorporate the feature where upon finding a name resides in a special purpose area of main storage, an interrupt to the processor causes invocation of an interrupt handler that performs a task of bringing the name level of from main storage to a physical register. This provides for additional computer registers and facilitates architectural features with overload architected register namespace reducing the overhead of register management without changing the instruction format of the computer by merely de-allocating and reallocating registers to/from memory.

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11. As per claim 9, Aizikowitz taught the memory hierarchy comprised and storage successively larger and slower in size (e.g., see col. 7, lines 52-65) and Bui taught a cache in the storage hierarchy (e.g., see col. 4, lines 13-23).

12. As per claims 17,18,19,20 Bui taught at least one of the registers is a physical register and an architected register and one of the new registers is a architected register (e.g., see col. 3, lines 1-66) and Aizikowitz taught memory includes a backing store (e.g., see col. 7, lines 38-65).

13. As per claims 21, Aizikowitz taught the name level instruction used for register spilling and Bui taught register spilling and hardware register renaming that maintains a pointer to a current physical register for a corresponding architected register(e.g., see col. 3, lines 1-67)[a backing store pointer storing the location of the first memory location of the current frame is created and stored in a register];

14. As per claim 22 Bui taught Providing a plurality of additional available computer registers without changing the format of the computer (e.g., see col. 3, line 60-col. 4, line 29)[allocates additional physical registers];.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ross (patent No. 6,314, 513) disclosed transferring data between a register stack and a memory resource (e.g., see abstract).

Bergner et al. (patent No. 6,523,173) disclosed allocating registers during code compilation using different spill strategies to evaluate spill cost (e.g., see abstract).

Tarditi (patent No. 6,925,639) disclosed a system for register allocation (e.g., see abstract).


Goebel (patent No. 5,901,316) disclosed a float register spill cache (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER